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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/910,915	07/24/2001	Kouji Yamamoto	IKE.008	2767

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EXAMINER	
ABRAHAM, ESAW T	

ART UNIT	PAPER NUMBER
2133	8

DATE MAILED: 04/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/910,915	YAMAMOTO, KOUJI	
	Examiner	Art Unit	
	Esaw T Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *# 6, 03/11/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Final rejection

Response to the applicant's amendments

******Amended drawings to correct minor spelling errors were received on 03/11/04 and accepted by the examiner.

******The corrected or amended claims 3 and 13 to overcome the rejection of 112-second paragraph are accepted by the examiner.

Response to the applicant's argument

Applicants argument with respect to original/amended claims have been fully considered but they are not persuasive. Therefore, the response in office action paper number 5 stands active or alive.

Response to remark pages 8-15, the applicant argues that there is no reason or teaching to combine the prior art (Kellogg) to the applicant's admitted prior art because Kellogg's system teaches an improvement to reliability of high performance of memory system not used to improve the speed of reading memory data. However, Kellogg's system further teaches to eliminate the need for extra parity memory chips for high performance memory systems with error checking capability (see col. 2, lines 8-12) which means eliminating extra memory chips would improve the speed of reading memory data. Therefore, the applicants' argument although acknowledged, has not been found to be convincing.

Further the applicant argues that Kellogg's ECC array is contrary to the claimed invention because Kellogg's system permits to dispose any location for the ECC array and it is possible to use a location far end similar to the applicant's admitted prior art. However, Kellogg in figure 3 element 164' disclose an ECC array other than far end and further based on the

applicant argument (any location for the ECC is acceptable), the examiner would like to point out that if the system of Kellogg accepted any location, that means it can also allow the ECC array to dispose in locations including other than far end or central. Therefore, the applied references have been applied appropriately.

DETAILED ACTION

1. Claims **1 to 20** are presented for examination.

Information Disclosure Statement

2. The examiner has been considered the references listed in the information disclosure statement submitted on 03/11/04 (see attached PTO-1449).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicants' submitted prior art in view of Kellogg et al. (U.S. PN: 6,070,262).

As per claims 1, 4, 11, 14-20, the applicants' admitted prior art in figure 3 substantially teach or disclose a conventional semiconductor memory device (ROM or RAM) having an ECC type error recovery comprises a memory cell array disposed in a matrix and each of cells arranged at an intersection a word line and bit line (digit line), a Y and X address decoders, an ECC circuit, a sense amplifier and an output circuit (see the applicants' disclosure, page 5, lines 18-25). The applicants' admitted prior art further teaches The ECC cell (see figure 3, the portion P1) disposed at the far end portion (see the applicants' disclosure, pages 5, last paragraph). The applicants' admitted prior art does not explicitly teach the ECC memory cell portion disposed at a location other than far end X decoder. However, Kellogg et al. teach in an analogous art teach that a DRAM array divided into two or more sub-arrays, with sub-array cells arranged in addressable rows and columns and further in normal mode and in ECC mode (see col. 2, lines 15-38). Furthermore, Kellogg et al. in figure 3 an ECC array arranged at the near end of the decoder (see element 164'). Therefore, it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to arrange the ECC memory location in different areas (locations) of the memory device as designed by Kellogg et al. This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so because disposing an ECC memory cell in different locations would heighten the decoding efficiency and increase the flexibility of configuration.

As per claims 2, 3, 12 and 13, the applicants' admitted prior art in view of Kellogg et al. teach all the subject matter claimed in claims 1 and 11 including Kellogg et al. in figure 3 teach element 164' an ECC array arranged at the near end of the decoder (see figure 3, element 164'). The admitted prior art in view of Kellogg et al. do not teach a specific location such as at the middle, or close (approximately) to the central. However, configuring the ECC cell array in different memory locations is common practice for most of error recovery systems. Therefore, it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to implement the ECC cell array in different memory locations. This modification would have been obvious because a person having ordinary skill in the art would have been motivated in order to heighten the decoding efficiency and increase the flexibility of configuration.

As per claim 5, the applicants' admitted prior art in view of Kellogg et al. teach all the subject matter claimed in claim 1 including the admitted prior art teach large number of memory cells (not showing in the drawings) disposed in a matrix (see the applicants' disclosure, page 5, lines 18-25).

As per claim 6, the applicants' admitted prior art in view of Kellogg et al. teach all the subject matter claimed in claim 1 including the admitted prior art teach a memory cell array disposed in a matrix and each of cells arranged at an intersection a word line and bit line (digit line), a Y and X address decoders (see the applicants' disclosure, page 5, lines 18-25 and fig. 3, elements 2 and 3).

As per claim 7, the applicants' admitted prior art in view of Kellogg et al. teach all the subject matter claimed in claim 1 including the admitted prior art teach an ECC circuit and an

ECC operation via sense amplifier and an output circuit (see the applicants' disclosure, page 5, lines 18-25 and fig. 3, elements 5 and 4).

As per claims 8 and 9, the applicants' admitted prior art in view of Kellogg et al. teach all the subject matter claimed in claim 1 including the admitted prior art in figure 3 teach or disclose a conventional semiconductor memory device (RAM or ROM) and further Kellogg et al. teach the semiconductor device is a RAM (see claim 1).

As per claim 10, the applicants' admitted prior art in view of Kellogg et al. teach all the subject matter claimed in claim 1 including the admitted prior art teach an ECC circuit and an output circuit (see the applicants' disclosure, page 5, lines 18-25 and figure 3, element 7).

4. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

5. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (703) 305-7743. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Esaw Abraham

Esaw Abraham

Art unit: 2133

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100